Circuit configuration and method of generating the drive signal of the deflection transistor of a cathode ray tube

The invention relates to a circuit configuration for generating the drive signal (HDRV = horizontal drive) for the deflection transistor that drives the oscillating circuit for the horizontal deflection of a cathode ray tube (CRT = cathode ray tube). The horizontal synchronization signal (HSYNC) and the horizontal flyback (HFB) are used as the input signals for the circuit configuration. The horizontal flyback is hereby proportional to the oscillating circuit voltage. Circuit configurations of this kind may be implemented as analog or digital.

The invention relates, in particular, to a circuit configuration that uses two phase-lock loops (PLLs). The first of these phase-lock loops hereby generates an internal, low-interference reference. The second of these phase-lock loops controls the phase angle of the loop "internal reference – horizontal drive (HDRV) – deflection transistor – oscillating circuit and horizontal flyback (HFB)". By contrast with the first control loop, this second control loop follows the dynamic, horizontal modulation, which is visible on the monitor by means of parallelogram setting, for instance. The second control loop has a very much smaller time constant T_{loop2}. It is known from the described circuit configuration for the generation of the drive signal of a deflection transistor and from other realizations that, in the ideal case, firstly, the horizontal position (hpos = horizontal position) and, secondly, the horizontal modulation (hmod = horizontal modulation) should each have an adjustment range of up to ±15%. A further, third requirement is that the horizontal duty time of the deflection transistor should be up to 60% and its storage time up to 30%. For example, approximately 2 msec storage time corresponds to 30% of the period at 140 kHz sweep frequency. In the known systems, all three of these requirements cannot be fulfilled. The overall coherence of the system means that an improvement of the value for one of the requirements leads to a deterioration of one of the other values.

The conventional circuit configuration for generating the drive signal for the deflection transistor has proved its worth, but the broad adjustment ranges required for the

horizontal position and the horizontal modulation in deflection transistors having long duty times and storage times cannot be achieved without increasing the back coupling of the second phase-lock loop by one period. This delaying of the reaction time would lead to a deterioration of the control response of the second phase-lock loop, and is generally not acceptable.

It is therefore the object of the invention to specify a circuit configuration which achieves the broad adjustment ranges required for the horizontal position and the horizontal modulation, even for a deflection transistor with a long duty time and storage time, without increasing the delay of the back coupling of the second control loop.

This object is achieved in accordance with the invention in that a first delay block is connected between the output of the first phase-lock loop and the input of the second phase-lock loop. The input signal of the delay block is the horizontal reference, and the output signal is a delayed, second horizontal reference, which is, in turn, an input signal of the second phase-lock loop. Together, the constant component of the first phase-lock loop and the constant component of the first delay block amount to more than 100%. The circuit configuration in accordance with the invention gives rise to a change in the phase measurement of the second phase-lock loop: the phase of the horizontal flyback is now measured against the delayed, second horizontal reference rather than against the single horizontal reference, as with the conventional circuit configuration.

The principle and advantage of the invention is that, for all horizontal positions (hpos) and horizontal modulations (hmod) together, i.e. for the range for hpos+hmod of –30% to +30%, the delayed, second horizontal reference lies between the occurrence of the horizontal flyback (HFB) and the start of the horizontal drive signal (HDRV) for the deflection transistor. This means that, following expiry of the horizontal flyback, the phase measurement can immediately proceed to the generation of the next horizontal drive signal (HDRV), and therefore a minimal delaying of the control loop (minimal loop latency) is achieved. With a required storage time of 60% and a duty time of 30%, it is thereby possible always to undertake phase measurement in the 10% slot remaining. The phase measurement thereby does not restrict the adjustment range of the horizontal modulation (hmod).

One further advantage of the circuit configuration in accordance with the invention is that the phase angle of the signals is always such that the phase detectors in the

two phase-lock loops initially measure the time of occurrence of the horizontal synchronization signal (HSYNC) and the horizontal flyback (HFB), then measure the time of occurrence of the first horizontal reference and the second horizontal reference, and finally produce the difference between these. The phase detectors are simplified as a result, especially in the case of digital implementations.

The invention will be further described with reference to examples of embodiments shown in the drawings, to which, however, the invention is not restricted.

Fig. 1 shows, in sub-figures a) and b), a block circuit diagram 1 of the circuit configuration in accordance with the invention with different control values.

Fig. 2 shows the signal waveform of the horizontal synchronization signal over time.

Fig. 3 shows the signal waveform of the horizontal reference over time.

Fig. 4 shows the signal waveform of the second horizontal reference over time.

Fig. 5 shows the signal waveform of the drive signal over time.

Fig. 6 shows the signal waveform of the horizontal flyback over time.

The signal waveforms in Figs. 2 to 6 represent the steady state.

The block diagram 1 of a two-PLL system shown in Fig. 1a) comprises a first phase-lock loop PLL1, a first delay block DB1, a second phase-lock loop PLL2, a second delay block DB2, and an RS flip-flop FF. An output of the first phase-lock loop PLL1 is connected to an input of the first delay block DB1. An output of the first delay block DB1 is connected to an input 2 of the second phase-lock loop PLL2. An output of the second phase-lock loop PLL2 is branched and led to an input S of an RS flip-flop FF and to an input of a second delay block DB2. An output of the second delay block DB2 is connected to an input R of the RS flip-flop FF. The two-PLL system described below is used, in particular, for the horizontal deflection of a cathode ray tube. Interface signals to the remaining system are the horizontal synchronization HSYNC, the drive signal HDRV for the deflection transistor and the horizontal flyback HFB. The drive signal HDRV, which is generated by the circuit configuration in accordance with the invention, switches the deflection transistor on and off.

The horizontal flyback HFB represents the position of the electronic ray on the monitor. Control values for the system shown are:

- for the first phase-lock loop PLL1:

as target phase ZP1: the horizontal position hpos, plus a constant component const1, which is generated in the first phase-lock loop and, in this embodiment example, is 30%, and

the quasi-static horizontal position, which is preset by the overall system, and is hpos = ±15%, so that ZP1 = 15% to 45%.

- for the delay block DB1:

as target phase ZP2: the dynamic horizontal modulation hmod, plus a constant component const2, which is generated in the first delay block and, in this embodiment example, is 80%, and

the horizontal modulation hmod, which is preset by the overall system, and is hmod = ±15%, so that ZP2 = 65% to 95%.

- for the second phase-lock loop PLL2:

as target phase ZP3: a constant component const3, which is generated in the second phase-lock loop and, in this embodiment example, is 10%, so that ZP3 also = 10%.

- for the second delay block DB2:

as target phase ZP4: the quasi-static horizontal duty time hduty, which is preset by the overall system, so that ZP4 = hduty = 40% to 60%.

The block diagram 1 shown in Fig. 1b) comprises the same elements as shown in Fig. 1a). The difference consists in the control values for delay block DB1 and the second phase-lock loop PLL2. In this embodiment example, control values for these are as follows:

- for delay block DB1:

as target phase ZP2: the first dynamic horizontal modulation hmod1 plus a constant component const2, which is generated in the first delay block and, in this embodiment example, is 80%, and

the first horizontal modulation hmod1, which is preset by the overall system and is hmod1 = ±14%, so that ZP2 = 66% to 94%.

- for the second phase-lock loop PLL2:

as target phase ZP3: the second horizontal modulation hmod2 plus a constant component const3, which is generated in the second phase-lock loop and, in this embodiment example, is 10%, and

the second horizontal modulation, which is preset by the overall system, and is hmod2 = ±1%, so that ZP3 = 9% to 11%.

In this embodiment example in accordance with Fig. 1b), adjustment of the horizontal modulation hmod takes place in two parts, hmod1 and hmod2, wherein hmod = hmod1+hmod2. It is preferred that the larger part hmod1 of, for example, +/- 14% is realized in the first delay block DB1, and the smaller part hmod2 of, for example, +/- 1% is realized in the second phase-lock loop PLL2. Owing to the division of the horizontal modulation, values that are especially suited to a digital implementation arise.

Fig. 2 shows the signal waveform of the horizontal synchronization signal HSYNC. A period interval identified as 100% starts and ends with the leading edge of a square-wave signal. The pulse duration is generally less than 25% and the leading edge or the center of the horizontal synchronization signal HSYNC is generally used as the reference point.

Fig. 3 shows the signal waveform of the internal, low-interference, horizontal reference HREF (= horizontal reference). The influence of target phase ZP1 of 15% to 45% on the output signal HREF of the first phase-lock loop PLL1 is shown with a dotted line. The square-wave pulse shown with a solid line illustrates the influence of constant component const1 = 30% in the case of hpos = 0%. The square-wave pulses at approximately 15% and approximately 45% show that the boundaries of the adjustment range of horizontal position hpos, which should fulfill the requirements of ±15%, have been reached, i.e. they are shifted 30% in order that they are only positive.

Fig. 4 shows the signal waveform of the delayed, second horizontal reference HREF2. In the example shown, the component, measured from the input signal HREF of delay block DB1 onwards, is const2 = 80%. This means that, in the case where hpos = 0% and hmod = 0%, viewed over a period interval of 100%, the leading edge of the square-wave signal of the second horizontal reference HREF2 appears at 10% of a period interval after the leading edge of the horizontal synchronization signal. This derives from formula 1:

$$30\%\ (HREF) + 80\%\ (HREF2) - 100\%\ (HSYNC) = 10\%\ (HFB) \qquad (1)$$

The maximum influence of the reference input variable hpos = ±15% is illustrated by the square-wave pulse shown with a dotted line to the right and left of the square-wave pulse shown with a solid line for hpos = 0%. The maximum effect of reference input variable hmod = ±15% is shown by the square-wave pulse shown with a dotted line to the right and left externally. The requirement for hmod can therefore be fulfilled in addition to the requirements for hpos, both requirements are ±15%.

Fig. 5 shows the signal waveform of the generated drive signal HDRV for the deflection transistor. The solid line shows the maximum pulse duration of 60%. The segments shown with dotted lines represent drive signal HDRV at a maximum pulse duration of 60% for the cases (hpos+hmod) = -30%, -15%, +15% and +30%.

Fig. 6 shows the signal waveform of the horizontal flyback HFB. In the example shown with a solid line, the horizontal flyback is in phase with the horizontal synchronization signal. Horizontal flyback HFB always appears with a delay constituting the storage time after switch-off of the deflection transistor (trailing edge of HDRV). Accordingly, the phase angle of horizontal flyback HFB varies in accordance with that of drive signal HDRV.

In a preferred embodiment of the invention, target phase ZP3 of the second phase-lock loop PLL2 is constant, e.g. 10%, and the horizontal modulation hmod is realized exclusively in target phase ZP2 of delay block DB1.

In a variant for operating the circuit configuration in accordance with the invention, target phase ZP2 for the first delay block DB1 lies in a range comprising the first part hmod1 and a constant component const2, so that ZP2 = hmod1 +80%. For hmod1, ±14% is preferably selected, thereby giving rise to a range from 66% to 94% for target phase ZP2. In addition, with this variant, target phase ZP3 for the second phase-lock loop PLL2 lies in a range formed from the second part and a constant component const3, so that ZP3 = hmod2 + 10%. For hmod2, ±1% is preferably selected, thereby giving rise to a range from 9% to 11% for target phase ZP3. This variant is particularly suited to digital implementation.

The circuit configuration in accordance with the invention generates a second horizontal reference signal HREF2, which, viewed over time, lies between the square-wave signal of the horizontal flyback and the square-wave signal of the drive signal for the deflection transistor for all horizontal positions hpos and horizontal modulations hmod together, i.e. for the range from hpos+hmod = -30% to hpos+hmod = +30%. For long storage times, e.g. $T_{STORAGE}$ = 30%, of the deflection transistor, and for long duty times, e.g. hduty = 60%, a time of 10% remains for the phase measurement and back coupling of the second phase-lock loop PLL2.

In summary, for the circuit configuration in accordance with the invention with a delay block DB1, a larger range for the horizontal modulation, more duty time and/or more storage time are acceptable for the positioning of the second horizontal reference signal HREF2 between the horizontal flyback HFB and the generated drive signal HDRV as

compared with the prior art, without extending the delay of the back coupling of the phase-lock loop to more than one period interval.